# Minimizing edge termination footprint in UHV SiC power devices: an area-efficient edge structure for power devices rated over 10 kV

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Ultra-High-Voltage (*UHV*) SiC devices are drawing attention as leading candidates for next-generation power systems, enabling performance advantages, topology simplifications and footprint reductions in the expanding market of MV high-power converters [1]. A critical aspect for UHV-SiC devices with blocking ratings exceeding 10 kV, is the design of effective edge-termination structures. Conventional edge structures with UHV blocking capabilities often entail large termination footprints. Such area consumption is particularly critical as UHV capabilities require the use of expensive SiC wafers with drift region thickness exceeding 100 µm [2]. Therefore, minimizing termination footprint while ensuring robust blocking performance is paramount for the commercialization of UHV-SiC devices. In this work, compact UHV terminations are investigated by TCAD simulations and designs achieving >10 kV blocking within a < 350 µm footprint are experimentally demonstrated.

Fig. 1 summarizes the concept and parameters of the termination of this work. This is a derivation the RA-JTE concept [3-4] where, differently from conventional design, high dose p-rings are used to enhance blocking capabilities. Table 1 summarizes the parameters of the four investigated designs (*D1-D4*). Fig. 2 compares the blocking capabilities extracted by TCAD for the investigated designs, comparatively to that of their constituent parts (rings and JTE only terminations), highlighting how the careful addition of p-rings in the JTE implant allows larger blocking voltages without increasing the footprint. The working principle of the terminations is further examined in Fig. 3. Fig. 3 (a) reports the electric field (*EF*) intensity in SiC as a function of the blocking voltage, showing that up to 10 kV all designs contain the maximum EF below the 2-2.5 MV/cm range. As further highlighted in Fig. 3(b), the EF peak is initially located at the JTE implant edge whereas, during the depletion of the main JTE implant at larger voltages, the p-rings get progressively engaged and the peak EF travels towards the active-transition overlap. Following the TCAD investigation, the terminations have been implemented in SiC-MOSFETs realized on 6-inch 4H-SiC wafers with a 100 µm thick epitaxial layer. A multi-mask approach has been employed to replicate the different termination designs on the same wafer. The implanted JTE dose has been varied across different wafers within a 50% range from the simulation optimal dose, while the p-ring dose has been fixed to a level that minimizes their depletion at increased blocking voltages. Experimental results are reported for the optimal dose only. The blocking capability of the MOSFETs has been characterized up to 10 kV directly at the wafer level. Fig. 4 exemplifies the blocking characteristics of MOSFETs employing D3 terminations. Within the investigated blocking range, the leakage current is mostly contained below 10 nA. Further experimental data is reported in Fig. 5. Fig. 5 (a) shows the cumulative distribution of the blocking voltage reached by the four designs ($V_{BD}$ defined at $I_{DS}(V_{DS})=1\mu A$). While for designs D1, D2 and D3, around 60% of the population exhibit a blocking voltage exceeding 10 kV, samples employing D4 design do not block over 3 kV, highlighting the role of the p-ring distribution in enhancing the blocking voltage and desensitizing the design from JTE dose variations. Fig. 5 (b) reports on the leakage current probability distribution for designs D1, D2 and D3, measured at 9 kV. On average, design D1 exhibits the lowest leakage current, with almost 70% of the population leaking less than 100 nA. Such result highlights the impact of the JTE width on the leakage current, where the reduced depletion area achieved by a smaller JTE allows to limit the average leakage current. Additional details and experimental characterization will be included in the final paper.

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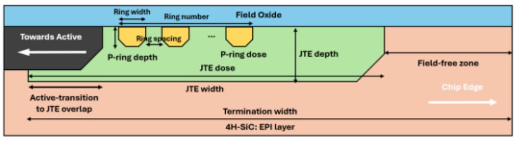


*Fig. 1 Termination concept and main design parameters.*

*Table 1. Summary of main variables of the investigated termination designs (D1-D4). The fixed size P-rings are spaced accordingly to the sequence $S_n = S_1+(n-1)S_i$,, where $S_1$ (initial ring spacing) and $S_i$ (ring spacing increment factor) are fixed for all designs.*

| Design | Termination width | JTE width | Field-free zone | P+ rings |
|---|---|---|---|---|
| Design 1 | 350 µm | 250 µm | 100 µm | 14 |
| Design 2 | 350 µm | 270 µm | 80 µm | 14 |
| Design 3 | 350 µm | 320 µm | 30 µm | 14 |
| Design 4 | 350 µm | 320 µm | 30 µm | 6 |

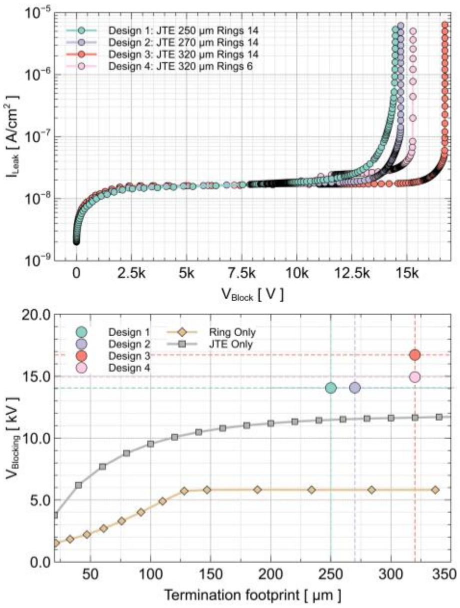


*Fig. 2 TCAD simulation results. (a) Blocking characteristics for designs D1-D4 at optimal JTE dose. (b) Simulated blocking voltage for D1-D4 compared to that of JTE ( at optimal dose) and Ring only (same ring distrbution as in D1-D4) terminations. The termination footprint is assumed as the width of the JTE implant or coordinate of the last p-ring.*

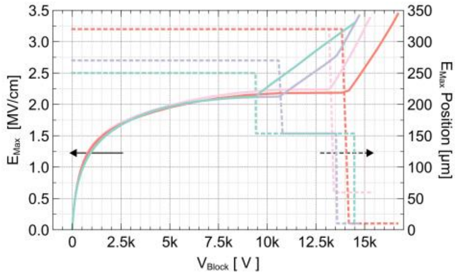
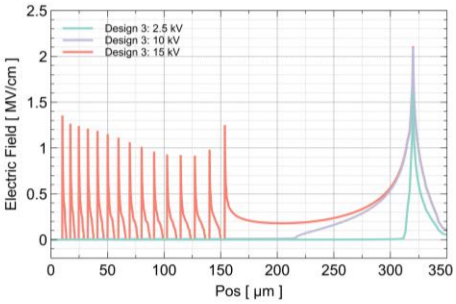


*Fig. 3 (a) Peak electric field in SiC and its location (expressed as distance from the active-transition overlap), as a function of the blocking voltage.*



*(b) Electric Field distribution at the SiC/FOX interface for D3, at different blocking voltages. Position (Pos) expressed as distance from the active-transition overlap.*

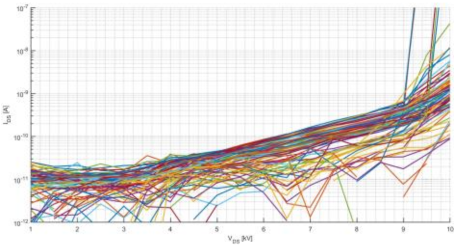


*Fig. 4 Wafer level forward blocking characteristics for MOSFETs implementing D3 termination design, measured at room temperature and $V_{GS}$=0.*

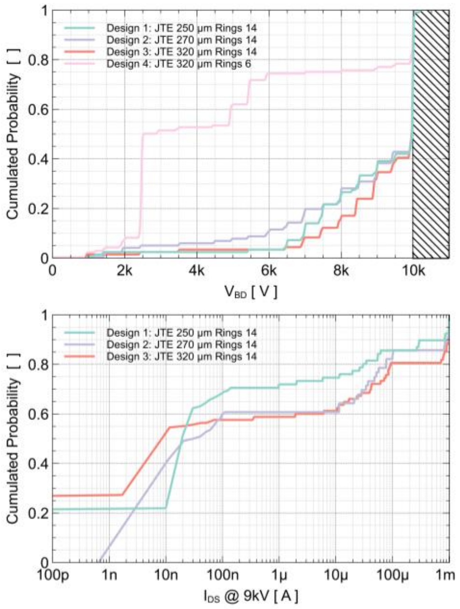


*Fig. 5 Cumulated probability distribution of the room temperature (a) blocking voltage measured at 1µA and (b) leakage current measured at 9 kV for designs D1-D4. Results are shown only for the optimal experimental JTE implanted dose.*

[1] D. Rothmund et al.,"99% Efficient 10 kV SiC-Based 7 kV/400 V DC Transformer for Future Data Centers," doi: 10.1109/JESTPE.2018.2886139

[2] N. Yun et al., "Developing 13-kV 4H-SiC MOSFETs: Significance of Implant Straggle, Channel Design, and MOS Process on Static Performance", doi: 10.1109/TED.2020.3017150.

[3] W. Sung et al., "A Comparative Study 4500-V Edge Termination Techniques for SiC Devices", doi: 10.1109/TED.2017.2664051.

[4] V. Soler et al., “Planar edge terminations for high voltage 4H-SiC power MOSFETs”, doi: 10.1088/1361-6641/aa52f0.